UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,504	05/08/2001	Theodore F. Vaida	01-036	2218

7590   03/08/2006

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EXAMINER
DUONG, DUC T

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/851,504	VAIDA ET AL.
	Examiner	Art Unit	
	Duc T. Duong	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>22 December 2005</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-7, 9-17 and 19-42</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) <u>21-42</u> is/are allowed.

6) ☒ Claim(s) <u>1-7, 10-17 and 20</u> is/are rejected.

7) ☒ Claim(s) <u>9 and 19</u> is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the
United States before the invention thereof by the applicant for patent, or on an international application
by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this
title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior

to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2.   Claims 1, 2, 8, 10-12, 18, and 20 are rejected under 35 U.S.C. 102(e) as being

anticipated by Brown et al (US Patent 6,347,347 B1).

Regarding to claims 1 and 11, Brown discloses a programmable network

application specific integrated circuit 16, comprising a media access controller 44

configured to transmit and receive network data via a physical interface device 24 (fig. 1

col. 3 lines 22-25); a programmable logic core 30 having array dynamically configurable

arithmetic logic units (fig. 1-2 col. 4 lines 36-47), said programmable logic core 30

configured to interface with said media access controller 44 and implement least one

application level function capable of generating meta-data (fig. 1-2 col. 6 lines 5-6; the

processor core 30 perform functions such as generate, store, or load address data (meta-data)).

Regarding to claims 2 and 12, Brown discloses the programmable logic core 30 may be programmed while said least one application level function executing (col. 6 lines 29-41).

Regarding to claims 3, and 13, Brown discloses the MP-block 16 comprising a data interconnect subsystem 14 configured to transmit and receive said network data from said MP-block (fig. 1 col. 3 lines 52-54) and a function master subsystem 12 configured to receive said meta-data from said MP-block and dynamically program said programmable logic units 30 (fig. 1 col. 4 lines 22-35).

Regarding to claims 4 and 14, Brown discloses the data interconnect system 14 is further configured to transmit and receive said network data from a host system (fig. 1 col. 3 lines 52-54).

Regarding to claims 5 and 15, Brown discloses the function master subsystem 12 is configured to transmit said meta-data to a host system and capable of receiving programming instructions from said host system (fig.1 col. 3 lines 55-60).

Regarding to claims 6 and 16, Brown discloses the function master subsystem 12 is capable of programming said programmable logic core based upon said meta-data (fig. 1 col. 3 lines 61-67 and col. 4 lines 1-5).

Regarding to claim 7 and 17, Brown discloses the function master subsystem 12 is capable of programming said programming logic core based upon said network data (fig. 1 col. 4 lines 6-12).

Regarding to claims 10 and 20, Brown discloses the programmable logic core includes a management interface 104 configured to control and manage said media access controller 44 (fig. 2 col. 5 lines 14-21).

Response to Arguments

3.   Applicant's arguments filed December 22, 2005 have been fully considered but they are not persuasive. Regarding to applicant's argument on pages 2-3, the processor core 30 in Brown fails to anticipate the claim limitation of "a programmable logic core having an array of dynamically arithmetic logic units". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the structure and function of an array of dynamically configurable logic units taught on pages 12-13 of the specification) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, in this instant the examiner construed the processor core 30 taught in Brown as a programmable logic core having an array of dynamically arithmetic logic units, see fig 2. col. 4 lines 36-47.

Allowable Subject Matter

4.   Claims 9 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5.   Claims 21-42 are allowed.

Conclusion

6.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Duc T. Duong whose telephone number is 571-272-

3122. The examiner can normally be reached on M-F (9:00 AM-6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Huy D. Vu can be reached on 571-272-3155. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

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DERRICK FERRIS
PATENT EXAMINER